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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,249	11/04/2003	Junji Ichimiya	2271/71388	6111

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EXAMINER	
TO, TUYEN P	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,249	ICHIMIYA, JUNJI	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/04/03; 03/08/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 11/04/2003. Claims 1-12 are pending.

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by **Hulse et al. (Hulse) (US Patent No. 6618847).**

Referring to claim 1, Hulse discloses the layout design method for a semiconductor integrated circuit, comprising the steps of:

providing a cell layout library which stores structure information of functional cells and a plurality of groups of filler cells (Abstract; col. 1, lines 58-60; col. 4, lines 11-24; col. 5, lines 9-15), each filler cell acting to fill space between the functional cells (Fig. 5-6, col. 1, lines 58-65), one of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal (col. 5, lines 25-43) wherein the lower-layer metal has a power rail and a ground rail which are not connected to the upper-layer metal (Fig. 6, element 25; col. 4, lines 58-65), and another of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal (col. 5, lines 25-43) wherein the lower-layer metal has a power rail and a ground rail (Fig. 6; col. 4, lines 58-65) one of which is connected to the upper-layer metal through a via

(col. 5, lines 25-43; using via to connect between different metal layers would have been a conventional technique, e.g. Zhen (US. Patent No. 6298468), col. 8, lines 54-58);

arranging the functional cells on a layout based on the structural information from the layout library(Fig. 2-5; col. 3, lines 48-67; col. 4, lines 1-24); and

arranging the filler cells of any of the plurality of groups selectively based on the structural information from the layout library (col. 1, lines 58+) so that the filler cells are arranged in channel regions where the functional cells are not located on the layout (Fig. 5, element 40; col. 4, lines 52-57; Fig. 6, element 25; col. 4, lines 58+), each channel region being located at a predetermined distance from signal lines on the layout (col. 3, lines 6-8 and 48-67).

Referring to claim 2, Hulse discloses the layout design method of claim 1 wherein the filler cells of at least one of the plurality of groups are arranged in the channel regions (Hulse; Fig. 5, element 40; Fig. 6, element 25) where standard cells and macro cells are not located on the layout, and power supply lines are arranged on the layout so that the filler cells of said at least one group are connected to the power supply lines (Fig. 6, col. 4, lines 58-65).

Referring to claim 3, Hulse discloses the layout design method of claim 1 wherein the filler cells of at least one of the plurality of groups which contain a bypass capacitor are arranged on the layout (abstract; col. 1, lines 64-66; col. 2, lines 4-9).

Referring to claim 4, Hulse discloses the layout design method of claim 1 wherein the filler cells of at least two of the plurality of groups have a common configuration with respect to intermediate layers between an uppermost layer and a lowermost layer of the layout (Fig. 8-9; col. 5, lines 7-43).

Referring to claim 5, Hulse discloses the layout design method of claim 1 wherein the filler cells are selectively arranged in the channel regions on the layout so that metal layers of the filler cells which are not connected to the signal lines are connected to power supply lines on the layout (Fig. 8; col. 4, lines 66+; col. 5, lines 1-15).

Referring to claim 6, Hulse discloses the layout design method of claim 1 wherein a duplicate arrangement of the filler cells of at least one of the plurality of groups is provided over a standard-cell region or a macro-cell region of the layout (Fig. 11A; col. 6, lines 12-22).

Referring to claim 7, Hulse discloses the semiconductor integrated circuit which is created by a layout design method using a cell layout library which stores structure information of functional cells and a plurality of groups of filler cells (Abstract; col. 1, lines 58-60; col. 4, lines 11-24; col. 5, lines 9-15), each filler cell acting to fill space between the functional cells (Fig. 5-6, col. 1, lines 58-65), one of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal (col. 5, lines 25-43) wherein the lower-layer metal has a power rail and a ground rail which are not connected to the upper-layer metal (Fig. 6; col. 4, lines 58-65), and another of the plurality of groups of filler cells containing an upper-layer metal and a lower-layer metal (col. 5, lines 25-43) wherein the lower-layer metal has a power rail and a ground rail (Fig. 6; col. 4, lines 58-65), one of which is connected to the upper-layer metal through a via (col. 5, lines 25-43; using via to connect between different metal layers would have been a conventional technique, e.g. Zhen (US. Patent No. 6298468), col. 8, lines 54-58), the semiconductor integrated circuit comprising:

the functional cells arranged on a layout based on the structural information from the layout library (Fig. 2-5; col. 3, lines 48-67; col. 4, lines 1-24);

signal lines arranged on the layout (*Fig. 10; col. 4, lines 25-35*) ; and

the filler cells of any of the plurality of groups selectively arranged based on the structural information from the layout library (col. 1, lines 58+) so that the filler cells are arranged in channel regions where the functional cells are not located on the layout (Fig. 5, element 40; col. 4, lines 52-57; Fig. 6, element 25; col. 4, lines 58+), each channel region being located at a predetermined distance from the signal lines on the layout (col. 3, lines 6-8 and 48-67).

Referring to claim 8, Hulse discloses the semiconductor integrated circuit of claim 7 wherein the filler cells of at least one of the plurality of groups are arranged in the channel regions (Fig. 5, element 40; Fig. 6, element 25) where standard cells and macro cells are not located on the layout, and power supply lines are arranged on the layout so that the filler cells of said at least one group are connected to the power supply lines (Fig. 6, col. 4, lines 58-65).

Referring to claim 9, Hulse discloses the semiconductor integrated circuit of claim 7 wherein the filler cells of at least one of the plurality of groups which contain a bypass capacitor are arranged on the layout (abstract; col. 1, lines 64-66; col. 2, lines 4-9).

Referring to claim 10, Hulse discloses the semiconductor integrated circuit of claim 7 wherein the filler cells of at least two of the plurality of groups have a common configuration with respect to intermediate layers between an uppermost layer and a lowermost layer of the layout (Fig. 8-9; col. 5, lines 7-43).

Referring to claim 11, Hulse discloses the semiconductor integrated circuit of claim 7 wherein the filler cells are selectively arranged in the channel regions on the layout so that metal layers of the filler cells which are not connected to the signal lines are connected to power supply lines on the layout (Fig. 8; col. 4, lines 66+; col. 5, lines 1-15).

Referring to claim 12, Hulse discloses the semiconductor integrated circuit of claim 7 wherein a duplicate arrangement of the filler cells of at least one of the plurality of groups is provided over a standard-cell region or a macro-cell region of the layout (Fig. 11A; col. 6, lines 12-22).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Hulse et al. (US Patent No. 6618847) disclose a layout design tool that allows designers to automatically intersperse filler cells around standard cell logic.

b) Law (US Patent No. 6691294) discloses a method and device for implementing by-pass capacitors to control ground bounce in semiconductor devices.

c) Zhen (US Patent No. 6298468) discloses a method and apparatus for optimizing pin placement.

d) Cano et al. (US Pub. No. 2002/0013931) disclose a method for power routing and distribution in an IC circuit with multiple interconnect layers.

e) McManus et al. (US Pub. No. 2003/0023935) discloses a method and apparatus for designing an integrated circuit with library cells.

f) Katsiouslas et al. (US Patent No. 6467074) discloses standard block architecture for integrated circuit design.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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